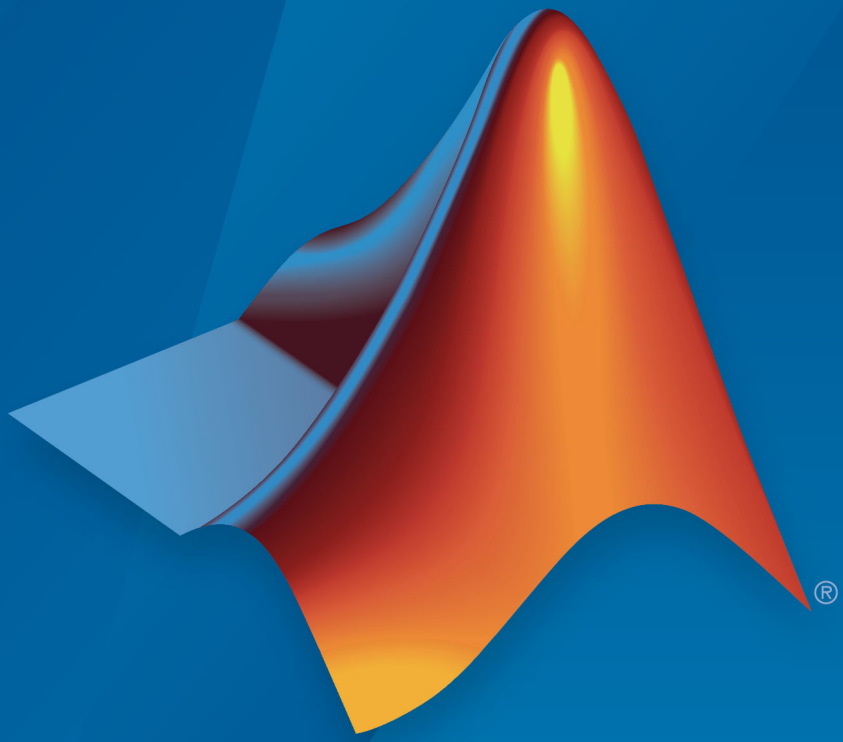
Mixed-Signal Blockset™

Getting Started Guide



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Revision History

March 2019	Online only	New for Version 1.0 (Release 2019a)

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Introduction to Mixed-Signal Blockset

Mixed-Signal Blockset Product Description

Design and simulate analog and mixed-signal systems

Mixed-Signal Blockset provides models of components and impairments, analysis tools, and test benches for designing and verifying mixed-signal integrated circuits (ICs).

You can model PLLs, data converters, and other systems at different levels of abstraction and explore a range of IC architectures. You can customize models to include impairments such as noise, nonlinearity, and quantization effects, and refine the system description using a top-down methodology.

Using the test benches provided, you can verify system performance and improve modeling fidelity by fitting measurement characteristics or circuit-level simulation results. Rapid system-level simulation using variable-step Simulink® solvers lets you debug the implementation and identify design flaws before simulating the IC at the transistor level.

With Mixed-Signal Blockset you can simulate mixed-signal components together with complex DSP algorithms and control logic. As a result, both analog and digital design teams can work from the same executable specification.

Introduction to PLL

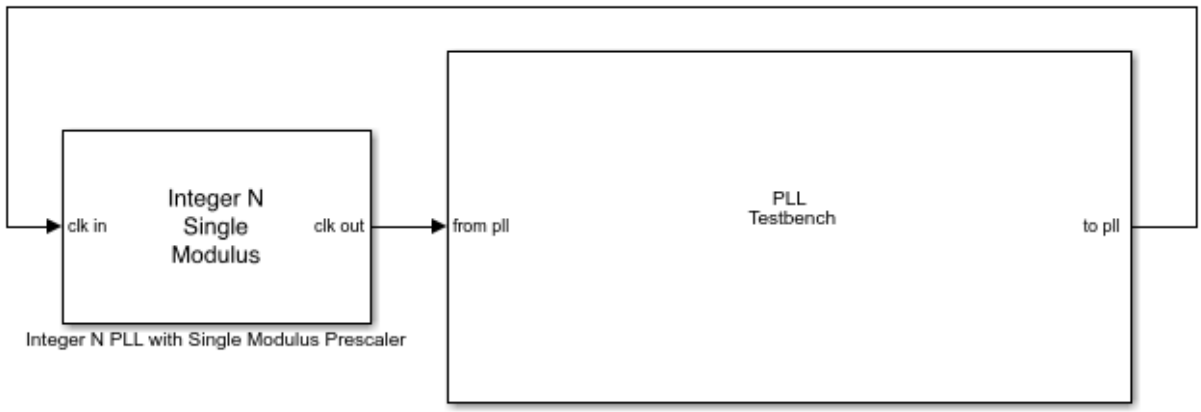
Design and Evaluate Simple PLL Model

This example shows how to design a simple PLL using a reference architecture, and validate the PLL using PLL Testbench.

Set UP PLL Testbench Model

Open the model `simplePLL`. The model consists of a Integer N PLL with Dual Modulus Prescaler and PLL Testbench.

```
open_system('simplePLL.slx')
```



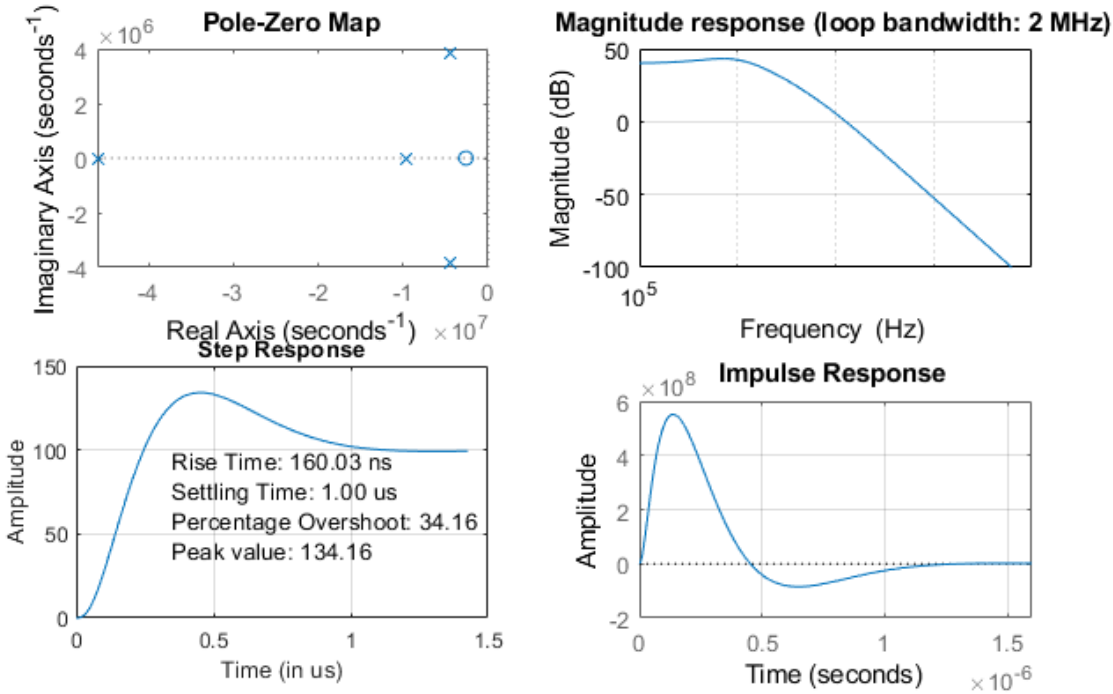
PLL Specifications and Impairment.

Double click the Integer N PLL with Dual Modulus Prescaler block to open the **Block Parameters** dialog box. Check that the impairments are enabled in the **PFD** and **Charge Pump** tabs. The effective clock divider value in the **Prescaler** tab is `70` . In the **Loop Filter** tab, **Filter component values** are calculated automatically. In the **Analysis** tab, both **Open Loop Analysis** and **Closed Loop Analysis** plots are selected.

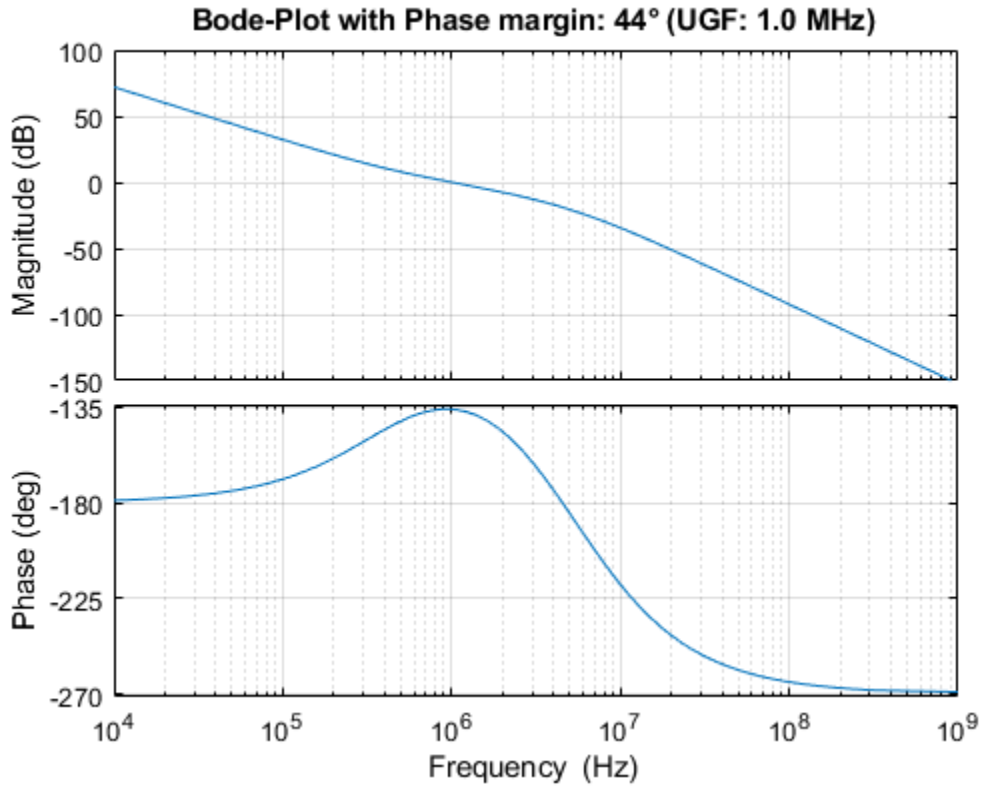
Plot Pre-Simulation PLL Loop Dynamics

Click the **Plot Loop Dynamics** button to view the pre-simulation results.

The closed loop analysis consists of the Pole-Zero Map, Magnitude Response, Step Response, and Impulse Response. The loop bandwidth of the system is 2 MHz.



The open loop analysis consists of Bode plots of the PLL system. The phase margin is 44 degrees.

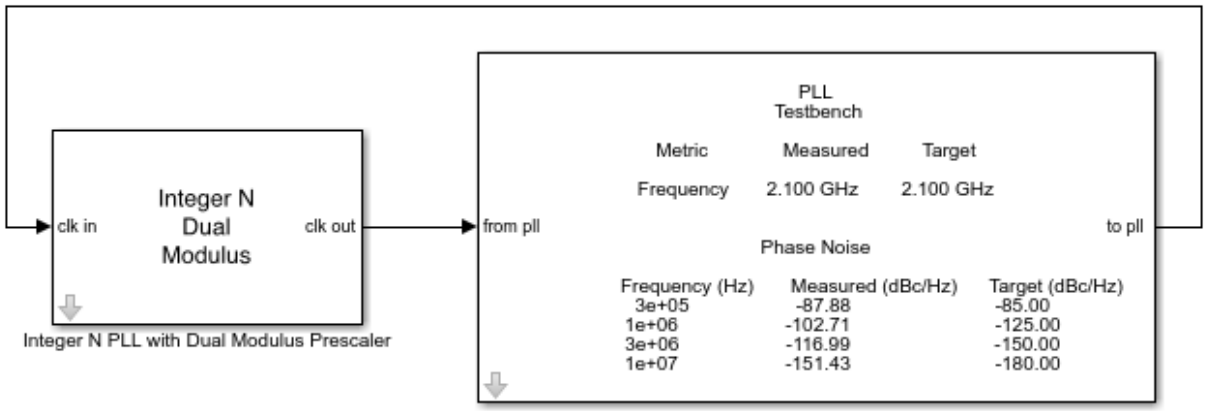


Modify PLL Testbench for Phase Noise Measurement

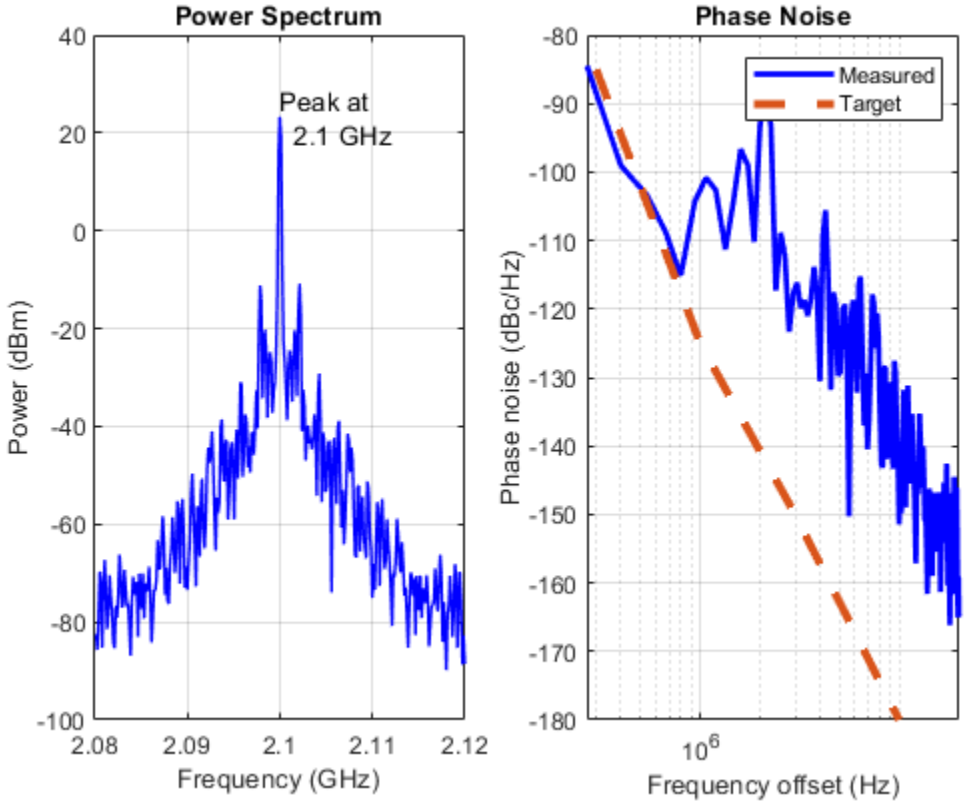
Double click the PLL Testbench to open the **Block Parameters** dialog box. In the **Setup** tab, check that the **Phase noise** measurement option is selected.

Plot PLL Phase Noise Profile

Run the simulation for `2.25e-5` s. The simulation results are displayed on the icon of the PLL Testbench. The measured phase noise levels at specific frequency offsets are in accordance with their target values.



Double click the PLL Testbench to open the **Block Parameters** dialog box. Click the **Phot phase noise** profile button. The PLL operating frequency is `2.1` GHz and the measured phase noise profile matches with the target profile.


Power Spectrum
Peak at
2.1 GHz
Power (dBm)
Frequency (GHz)
40
20
0
-20
-40
-60
-80
-100
2.08
2.09
2.1
2.11
2.12
Phase Noise
Measured
Target
Phase noise (dBc/Hz)
Frequency offset (Hz)
-80
-90
-100
-110
-120
-130
-140
-150
-160
-170
-180
10^6

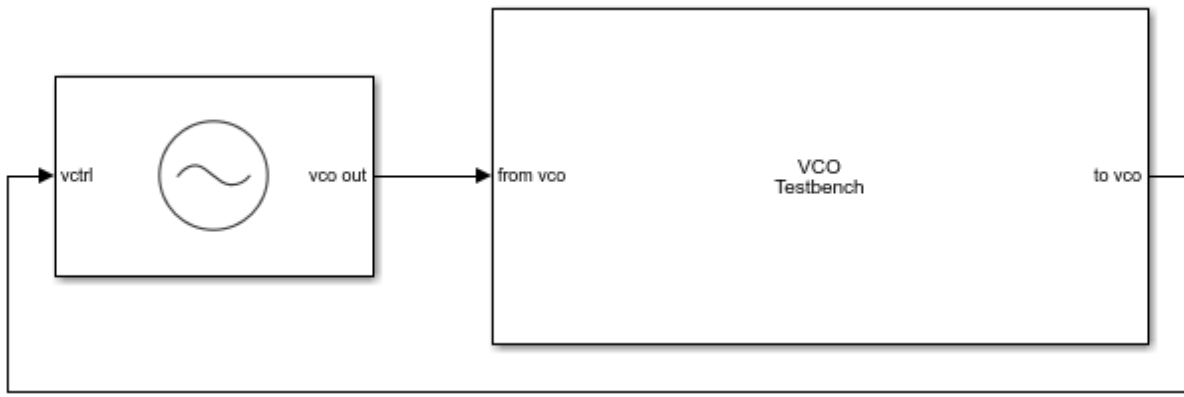
Phase Noise Analysis in VCO

This example shows how to measure and analyze the effect of phase noise in a voltage controlled oscillator (VCO). Using a VCO block and VCO testbench, this example defines the typical phase noise levels from datasheet specifications and validates the VCO.

Set Up VCO Testbench Model

Open the model `vcoPhaseNoiseAnalysis` . The model consists of a VCO block and a VCO Testbench.

```
open_system('vcoPhaseNoiseAnalysis.slx')
```



VCO Specifications and Phase Noise Impairments

Double click the VCO block to open the **Block Parameters** dialog box. In the **Configuration** tab, the **Voltage Sensitivity (Hz/V)** is set to `125e6`. In the **Impairment** tab, check that the **Add phase noise** option is enabled. **Phase noise frequency offset (Hz)** and **Phase noise level (dBc/Hz)** parameters represent a typical phase noise profile in a VCO.

Modify VCO Testbench According to VCO Specifications

Double click the VCO Testbench block to open the **Block Parameters** dialog box. In the **Stimulus** tab, **Control voltage (V)** is set to `4`.

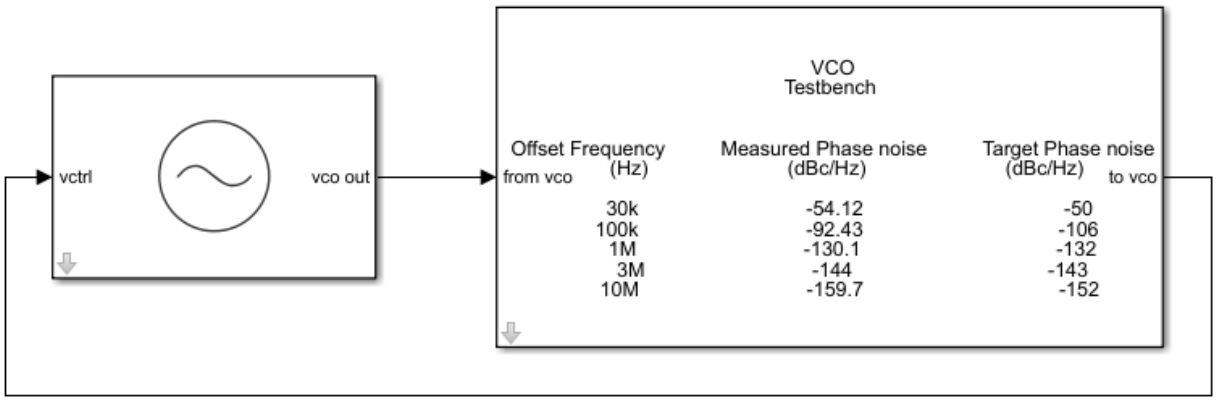
Since the VCO has a sensitivity of `1` MHz/V and the free running frequency of `2.5` GHz, the operating frequency of the VCO is `3` GHz. In the **Setup** tab, the **Sampling frequency**

(Hz) is set to `24e9`, which is eight times the target operating frequency. Also check that in the **Target Metric** tab, the **Phase noise frequency offset (Hz)** and **Phase noise level (dBc/Hz)** parameters match the values set in the VCO block.

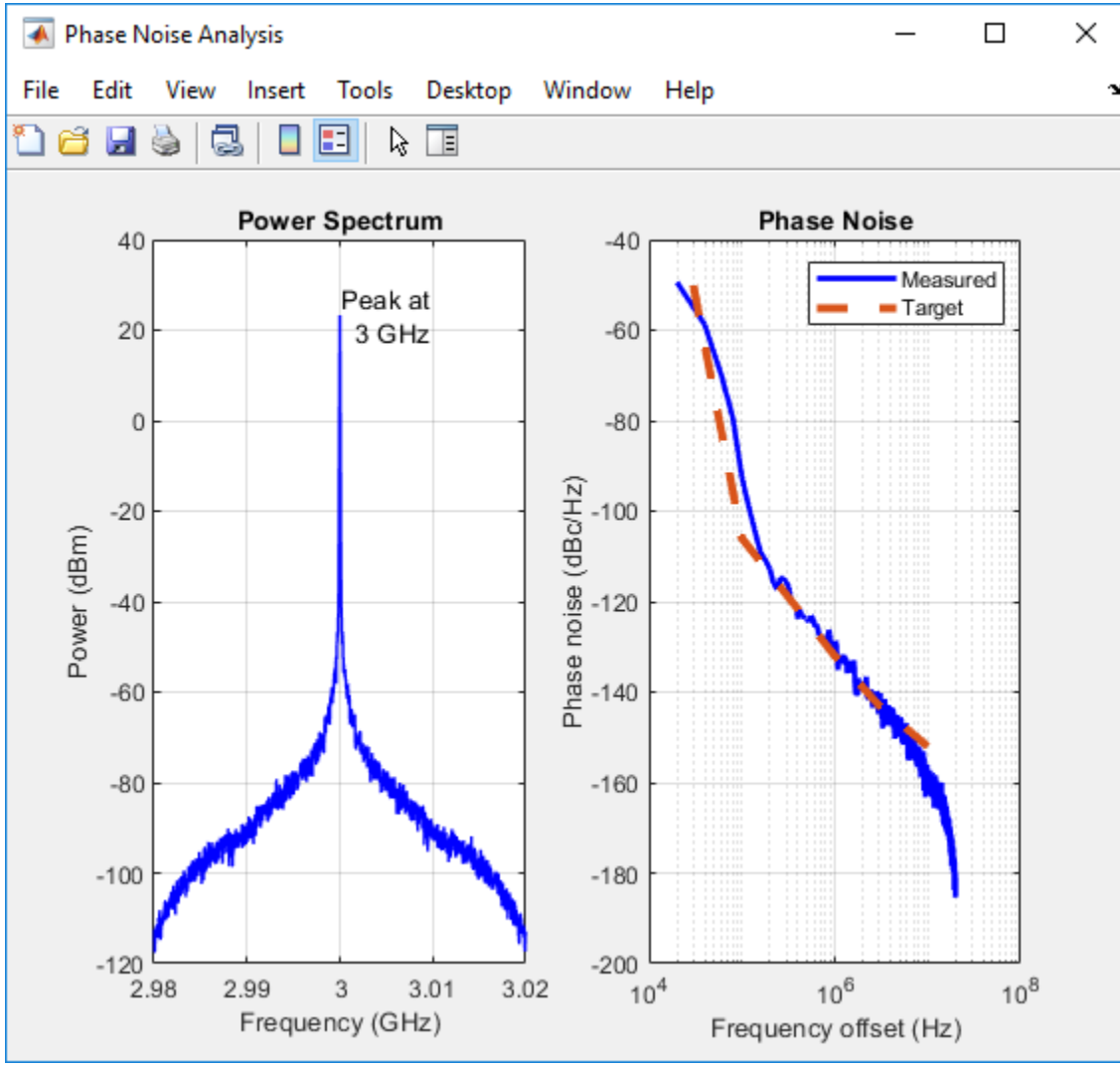
Plot Phase Noise Profile

Run the simulation for `1.2` ms, according to the **Recommmended min. simulation stop time (s)** in the **Block Parameters** dialog box of VCO Testbench.

Once the simulation is complete, the phase noise profile is displayed on the icon of the VCO Testbench. The measured phase noise is comparable to target phase noise.



In the **Block Parameters** dialog box of VCO, click the **Plot measurement** button to plot the phase noise profile of the VCO. Notice that the VCO operating frequency is 3 GHz, and that the measured and targeted phase noise profiles match.


Phase Noise Analysis
File Edit View Insert Tools Desktop Window Help
Power Spectrum
Peak at
3 GHz
Power (dBm)
Frequency (GHz)
Phase Noise
Measured
Target
Phase noise (dBc/Hz)
Frequency offset (Hz)

3

Introduction to ADC

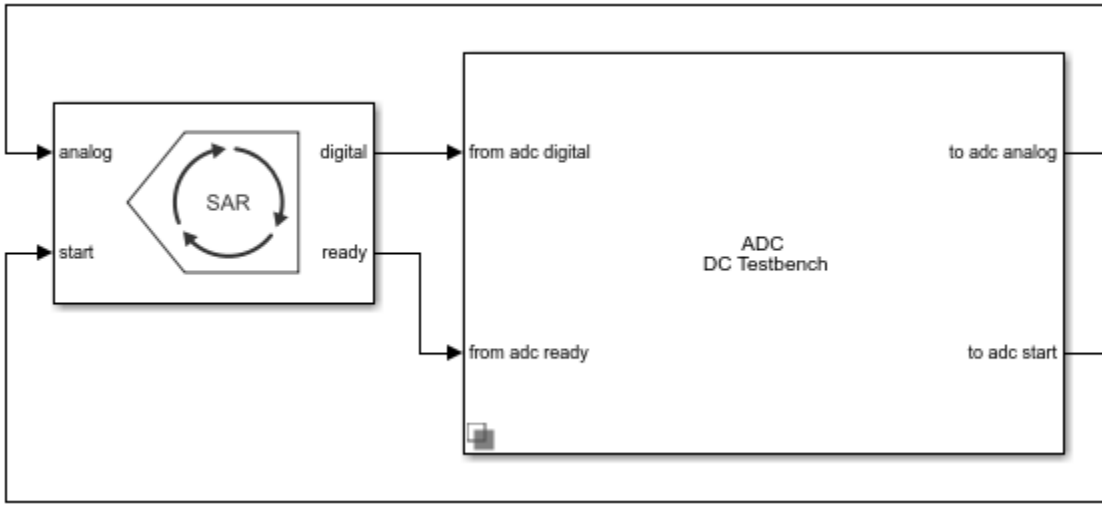
Design and Evaluate a SAR ADC

This example shows how to design a SAR ADC using reference architecture and validate the ADC using ADC Testbench.

Set UP SAR ADC Testbench Model

Open the model SAR_ADC attached to this example as a supporting file. The model consists of a SAR ADC block and an ADC Testbench.

```
open_system('SAR_ADC.slx')
```



ADC Specifications and Impairmenta

Double click the SAR ADC block to open the Block Parameters dialog box. The **Number of bits** is set to 8, and the **SAR Frequency** is 2e7 Hz. Check that in the **Impairments** tab, impairments are enabled.

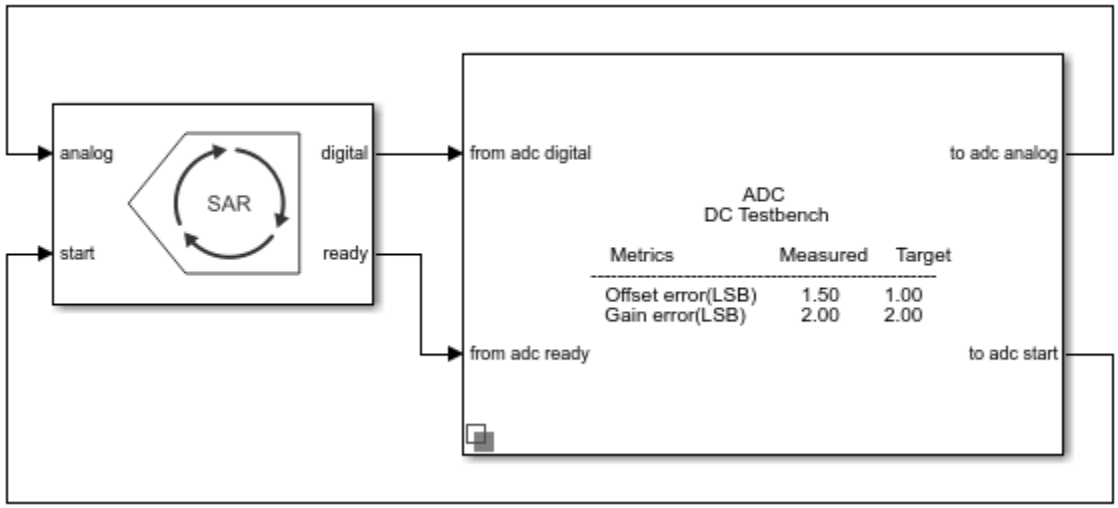
Modify ADC Testbench According to ADC Specification

Double click the ADC Testbench block to open the Block Parameters dialog box. The **Measurement** option is selected as DC. In the **Setup** tab, click the **Autofil setup parameters** button to automatically propagate the ADC parameters to the testbench. In

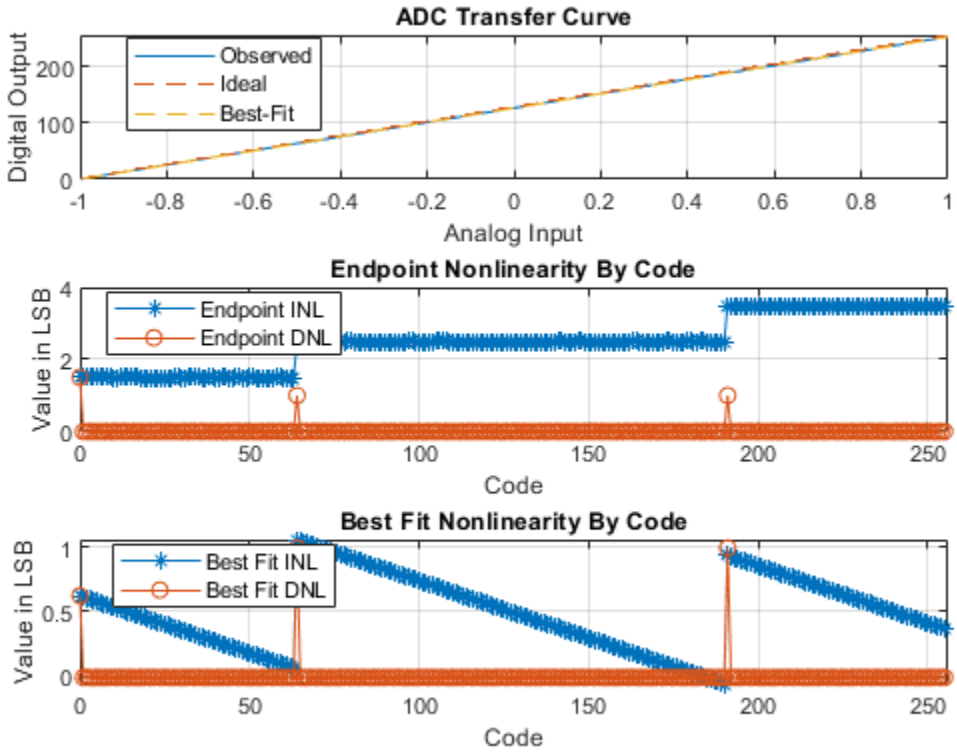
the **Target Metric** tab, click the **Autofil target metric** button to automatically propagate the ADC target metrics to the testbench. Save the changes.

Plot DC Analysis Results

Run the simulation for `0.00512` s. The measured and target values of offset error and gain error are displayed on the icon of the ADC Testbench block.



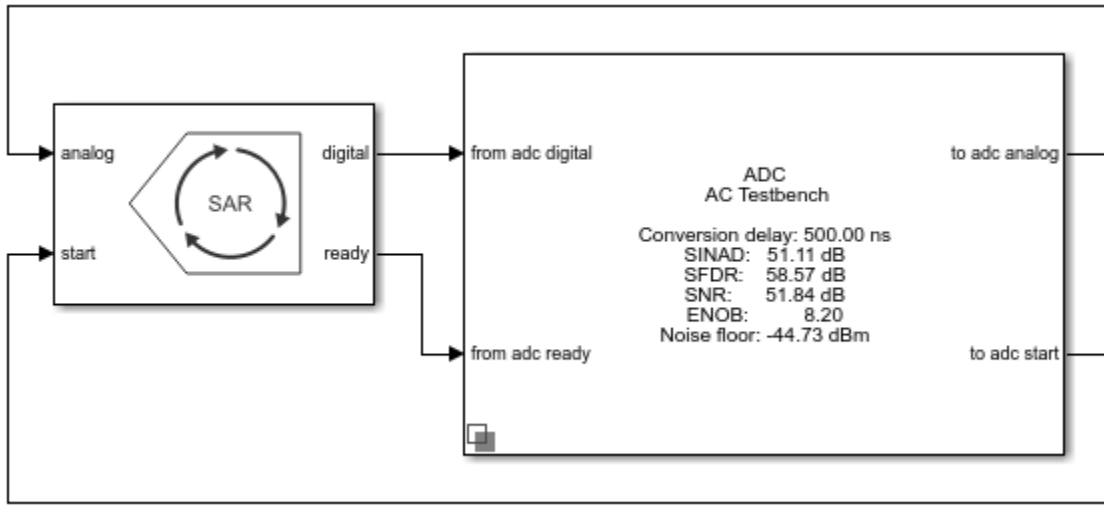
Double click the ADC Testbench block to open the Block Parameters dialog box. Click the **Plot DC analysis results** button to view the ADC transfer curve, endpoint nonlinearity and best fit nonlinearity.



Perform AC Analysis

Double click the ADC Testbench block to open the Block Parameters dialog box. Set the *Measurement option to `AC` and save the change.

Run the simulation for `0.009` s. The conversion delay, SINAD, SFDR, SNR, ENOB and Noise floor are displayed on the icon of the ADC Testbench.


analog
start
SAR
digital
ready
from adc digital
from adc ready
ADC
AC Testbench
Conversion delay: 500.00 ns
SINAD: 51.11 dB
SFDR: 58.57 dB
SNR: 51.84 dB
ENOB: 8.20
Noise floor: -44.73 dBm
to adc analog
to adc start